IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

 Applicant:
 Aggarwal et al.
 Art Unit:
 2811

 Serial No.:
 10/828,446
 Examiner:
 Crane, S.

 Filing Date:
 04/20/2004
 Docket No.:
 TI-36296

 Customer No.:
 23494
 Conf. No.:
 4009

Title: A FERROELECTRIC CAPACITOR HAVING AN OXIDE ELECTRODE
TEMPLATE AND A METHOD OF MANUFACTURE THEREFOR

RESPONSE AFTER FINAL

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

The following remarks are offered in response to the Examiner's Office Action dated November 15, 2006. They are respectfully submitted as a full and complete response to that Action.

REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 1-8, 10, 21, and 22 are pending in this case.

The Examiner rejected claims 1-8, 10 and 21 under 35 U.S.C.§ 103(a) as being unpatentable over Inoue et al. in view of Ko et al., and further in view of Nishihara et al., Hidecki, and Jia et al.

Applicant respectfully submits that claim 1 is patentable over the references as there is no disclosure or suggestion in the references of a first electrode layer located over a substrate, wherein the first electrode layer includes iridium, an oxide electrode template located over the first electrode layer, and a ferroelectric dielectric layer located over the oxide electrode template, wherein the oxide electrode template and the ferroelectric dielectric layer have substantially similar crystal structures. Inuoe, taken as a whole, teaches an adhesion layer below a lower electrode 109 and a ferroelectric dielectric 110 formed on the lower electrode. Inoue further teaches that the lower electrode may comprise Pt, Ir, or IrO2. Inoue does not teach an oxide electrode template located between the lower electrode and the ferroelectric dielectric, much less one having a substantially similar crystalline structure to the ferroelectric dielectric. The ferroelectric dielectric 110 in Inoue is located directly on the lower electrode 109. Similarly, Ko teaches forming the ferroelectric dielectric directly on the Pt layer of the lower electrode. Nishihara teaches a variety of electrode materials with the ferroelectric dielectric formed directly on the lower electrode. None of the references disclose or suggest placing an oxide electrode template having substantially similar crystalline structure to the ferroelectric dielectric between the lower electrode and the ferroelectric dielectric. Only Inoue teaches a layer in addition to the lower electrode. However, that layer is an adhesion layer 108 located below the lower electrode.

Furthermore, while the references taken together teach a variety of electrode materials, they do not disclose or suggest using an oxide electrode template having a substantially similar crystalline structure to the ferroelectric dielectric in addition to a lower electrode comprising Ir. While Nishihara teaches using SrIrO or SrRuO₃ as a lower electrode, there is no disclosure or suggestion for using either of these materials in conjunction with an Ir comprising lower electrode, as required by the claim.

Appl. No. 10/828,446 Reply to Office action of 11/15/2006

Accordingly, Applicant respectfully submits that claim 1 and the claims dependent

thereon are patentable over the references.

Applicant respectfully submits that claim 21 is similarly patentable over the

references.

The Examiner rejected claim 22 under 35 U.S.C. 103(a) as being unpatentable

over references as applied to claim 20 above, and further in view of Goo et al.

Applicant respectfully submits that claim 22 is patentable over the references for

the same reasons discussed above relative to claim 21 from which claim 22 depends.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's

rejections and allowance of claims 1-8, 10, 21, and 22. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that

the Examiner contact Applicant's attorney at the below listed telephone number and

address.

Respectfully submitted.

/Jacqueline J Garner/

Jacqueline J. Garner

Reg. No. 36,144

Texas Instruments Incorporated P. O. Box 655474, M.S. 3999 Dallas, Texas 75265

Phone: (214) 532-9348 Fax: (972) 917-4418

-3-